Nonvolatile Resistive Switching in $Pt/LaAlO_3/SrTiO_3$ Heterostructures

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Resistive switching heterojunctions, which are promising for nonvolatile memory applications, usually share a capacitorlike metal-oxide-metal configuration. Here, we report on the nonvolatile resistive switching in $Pt/LaAlO_3/SrTiO_3$ heterostructures, where the conducting layer near the $LaAlO_3/SrTiO_3$ interface serves as the ''unconventional'' bottom electrode although both oxides are band insulators. Interestingly, the switching between low-resistance and high-resistance states is accompanied by reversible transitions between tunneling and Ohmic characteristics in the current transport perpendicular to the planes of the heterojunctions. We propose that the observed resistive switching is likely caused by the electric-field-induced drift of charged oxygen vacancies across the $LaAlO_3/SrTiO_3$ interface and the creation of defect-induced gap states within the ultrathin $LaAlO_3$ layer. These metal-oxide-oxide heterojunctions with atomically smooth interfaces and defect-controlled transport provide a platform for the development of nonvolatile oxide nanoelectronics that integrate logic and memory devices.

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I. INTRODUCTION

Heterostructures of perovskite oxides are emerging as one of the most fascinating systems in condensed-matter physics, exhibiting a wide range of properties [1], such as the two-dimensional electron gas [2–4], orbital reconstruction [5,6], interfacial superconductivity [7,8], ferromagnetism [9–11], and enhanced capacitance [12]. In particular, the discovery of high-mobility conduction at the interface between two insulators $LaAlO_3$ (LAO) and $SrTiO_3$ (STO) has launched intensive experimental and theoretical investigations on the physics and applications of this novel strong correlated electronic state [2–4,13,14]. Upon its discovery, the interfacial electron system was linked with the scenario of electronic reconstruction [2,15], where half an electron per Ti ion is transferred across the LAO/STO interface as a result of polar discontinuity at the polar-nonpolar interface, forming the electron system. This mechanism, along with the polar distortion and dipole screening in the LAO overlayers [16], can qualitatively explain the transport properties. In addition, factors like oxygen vacancies [17–19] and cation mixing [20–22] may influence the characteristics of the electron gas [23–27].

Transport in the direction perpendicular to the planes of the metal/LAO/STO heterojunctions, which we refer to as current-perpendicular-to-plane (CPP) transport in what follows, has been less investigated compared to the current-in-plane (CIP) case. In fact, the conducting region near the LAO/STO interface can serve as the bottom electrode in such heterojunctions; in particular, good conduction in a reduced STO surface layer can be achieved when the thin-film growth takes place at low oxygen pressures. In ultrathin heterostructures, applied voltage bias corresponds to an enormous electric field on the scale of 10^7 V/cm or higher, which is high enough to drive not only electronic processes but also motions of ionic species, in particular, charged oxygen vacancies. Therefore, it is interesting to question how the physical properties of such heterostructures will respond to such an enormous electric field. Ultrathin heterostructures offer unprecedented opportunities for the investigation of concurrent electronic and ionic phenomena. First-principles calculations, which are difficult to implement in conventional junctions with thick films as a result of computational limitations, can yield valuable information on the underlying physics in unit-cell-thin systems.

Here, we report on a Pt/LAO/STO memory device that may not only serve in oxide electronics [Fig. 1(a)] but also shed light on the coupled electronic and ionic processes in ultrathin heterostructures. In logic devices like field-effect

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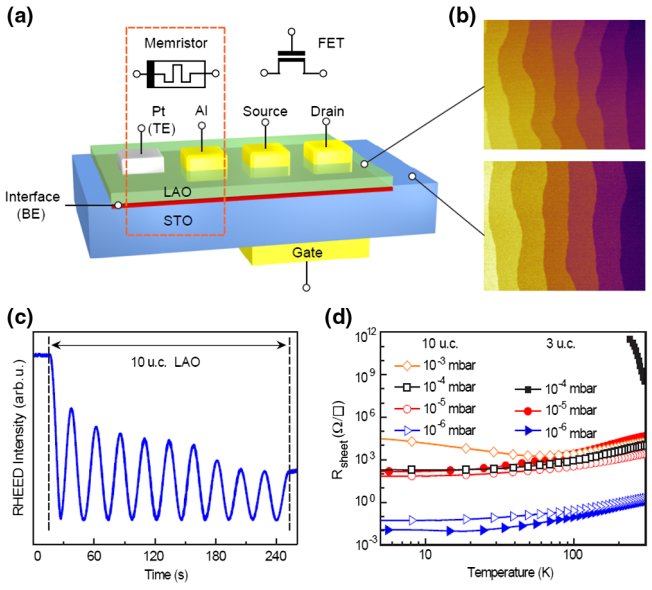

FIG. 1. (a) Proposed scheme of integrating both the high-performance memristor and field-effect transistor at the oxide interfaces. The conducting interface that serves as the bottom electrode is contacted using Al wire bonding. A positive bias is defined as current flowing from the top Pt electrode into the device. (b) Atomic-force-microscopy images taken on the TiO_2-terminated STO substrate as well as after the growth of 10-u.c. LAO. (c) Typical RHEED oscillation observed *in situ* during the PLD thin-film growth. (d) Temperature dependence of sheet resistance measured for the *n*-type LAO/STO interface in 3- and 10-u.c. LAO films grown at various partial oxygen pressures.

transistors (FET), the carrier concentration of the channel is tuned electrostatically. Thiel *et al.* reported a room-temperature field-effect modulation of the LAO/STO interface [the back-gate FET is illustrated in Fig. 1(a)], with a three-unit-cell (u.c.) insulating interface that can be switched into a metallic state by the gate bias [3]. Advancing toward nanodevices, it has been recently demonstrated that the LAO/STO interface can be reversibly switched between insulating and conducting states by locally sketching with a biased conducting atomic-force-microscope tip [28,29]. Besides logic FET, memory devices are the other vital component of integrated nanoelectronics. A resistive switching (RS) device has electronic conduction that can be switched between nonvolatile "ON" (low-resistance) and "OFF" (high-resistance) states in the CPP configuration [30–34]. In fact, these RS systems represent a particular class of dynamic circuit element known as the "memristor" [35,36]. Although some previous experiments revealed certain memorylike effects at the LAO/STO interface [3,28,29,37], three-terminal FET structures or conducting atomic-force-microscope tips were involved. For example, persistent conduction was observed in FET even after the gate voltage was removed, which was attributed to trap states in STO [3]. On the other hand, the conventional RS memories generally have a capacitorlike device structure with two electrodes. So far, there has been no report on the employment of LAO/STO heterostructures in two-terminal nonvolatile RS devices, which in turn restrains our understanding on the CPP transport in such ultrathin oxide heterostructures.

In this work, we demonstrate RS devices based on Pt/LAO/STO heterostructures, which may enable the potential integration of memory and logic devices in the monolithic entity of interface-based oxide nanoelectronics [Fig. 1(a)]. Different from conventional RS devices that use metal layers as electrodes in the metal-oxide-metal configuration, in our scheme, we employ the conducting layer near the oxide interface as the bottom electrode (BE), and the voltages applied to the top electrode (TE) of Pt accomplish the RS across the Pt/LAO/STO heterojunctions. Importantly, the drastic modification of the CPP transport and the reliable control underline such ultrathin heterostructures as a model system to investigate the physics of complex oxides under a high electrical stress. Our complementary experimental and calculation results confirm that the electric-field-driven motions of oxygen vacancies across the LAO/STO interface dictate the CPP transport of such heterostructures. This scheme of constructing nonvolatile memories based on metal-oxide-oxide heterostructures complements the existing metal-oxide-metal configuration while providing new insights on the physical properties of ultrathin oxide heterostructures.

II. SAMPLE FABRICATION

To obtain the conducting bottom electrode near the LAO/STO interface, we grow LAO thin films with thicknesses from 3 to 30 u.c. on TiO_2-terminated $SrTiO_3(001)$ substrates using pulsed laser deposition (PLD) at 800 °C. The repetition rate of the KrF laser is 1 Hz, and the fluence is 1 J/cm^2. The atomic-force-microscopy images in Fig. 1(b) taken both before and after the growth exhibit atomically smooth surfaces with clear unit-cell-height steps. The film growth is monitored by *in situ* high-pressure reflection high-energy electron diffraction (RHEED) as previously reported [38,39], and the intensity oscillations [Fig. 1(c)] indicate a layer-by-layer growth mode. As the oxygen stoichiometry is one of the most important factors determining the physical properties of oxide interfaces, we grow LAO films on STO substrates in a wide range of P_{O2} from 10^{-6} to 10^{-3} mbar.

The CIP transport properties of the LAO/STO heterostructures without the top metal contacts are measured in a physical property-measurement system (Quantum Design) using the Hall-bar geometry. The temperature-dependent sheet resistance data of the samples are shown in Fig. 1(d). Typically, the 10-u.c. samples exhibit metallic behavior regardless of the growth pressure. On the other hand, insulating behavior is observed in the 3-u.c. samples

when the growth pressure is higher than 10^{-4} mbar, consistent with earlier reports [9]. Samples are metallic when the growth pressure is below 10^{-5} mbar. In such a highly reducing environment, a high density of oxygen vacancies is generated; thus, even the 3-u.c. LAO samples exhibit metallic transport behavior. Based on these transport data, we can conclude that oxygen vacancies play a key role in the conduction of low-pressure-grown samples by contributing high-density electrons near the interface [18]. The presence of oxygen vacancies causes the carrier distribution to extend deep into the STO substrate [25]. In contrast, a two-dimensional nature of the interface transport can be achieved in high-pressure-grown samples, with the electrons being confined a few nanometers near the interface. These transport results are consistent with previous reports on properly oxidized LAO/STO heterostructures [24–26]. It is noteworthy that we do not perform any postdeposition annealing in our sample synthesis; thus, as suggested in a recent study [27], oxygen vacancies exist in even the high-pressure-grown samples and their contribution to the transport of LAO/STO heterostructures cannot be ignored.

To further characterize our Pt/LAO/STO heterostructures, we carry out high-angle annular dark-field scanning transmission-electron-microscopy (HAADF-STEM) measurements. More details can be found in the Appendix. Figure 2(a) shows an overview image of the as-grown heterostructure. Under the HAADF-STEM imaging conditions used, the image contrast is approximately proportional to $Z^{1.7}$, yielding a heightened image contrast for the Pt layer and the LAO layer with respect to the STO substrate. In the high-resolution image in Fig. 2(b), the interface between the LAO layer and the Pt contact appears to be slightly wavy, but the overall structural integrity of the LAO layer remains intact and there is no sign of Pt diffusion into the LAO layer. Naturally, TEM provides only very local structural information and does not provide details on possible thickness variations over a long range of hundreds of microns. However, as the sample for STEM observation is prepared using a focused ion beam from a random site under the Pt electrodes on the sample, there is no reason to believe that any major structural differences are present in other regions. On the other hand, as shown in Fig. 2(b), the uppermost unit cell of LAO appears discontinuous, indicating a certain degree of thickness fluctuation in the LAO layer. In addition, we cannot exclude the possibility of damage to the top LAO layer of 1 or 2 u.c. as a result of the Pt deposition, and a certain degree of cation mixing at the LAO/STO interface was also proposed in the literature [20–22]. The epitaxial cube-on-cube growth of the LAO layer on the STO substrate is confirmed by the Fourier-transform pattern in the inset taken from the layer and the substrate simultaneously. The interface between the LAO layer and the STO substrate is atomically flat, as indicated by arrows in Fig. 2(c). No dislocations or other defects are found to be present at the LAO/STO interface.

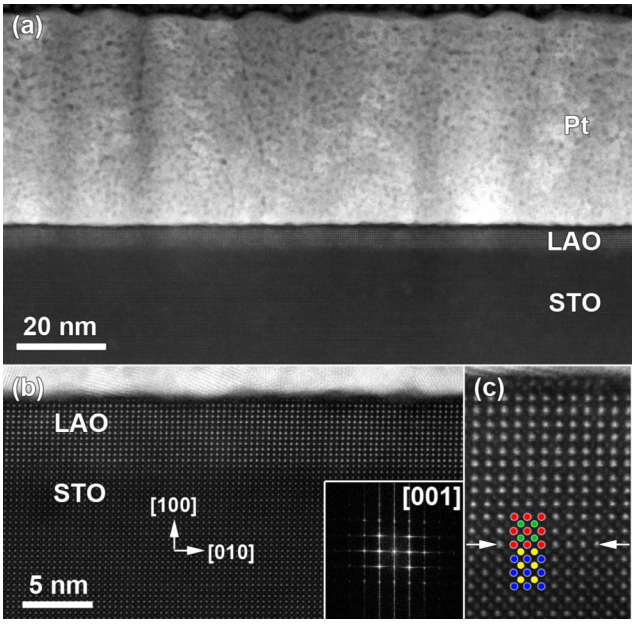

FIG. 2. (a) Overview and (b) high-resolution HAADF-STEM images of a Pt/LAO/STO heterostructure. A Fourier-transform pattern taken from the LAO layer and STO substrate simultaneously confirms the cube-on-cube growth, imaged along the 001 zone axis orientation. (c) High-resolution image of the LAO/STO interface, which is marked by arrows. In the atomic overlay, La positions are marked in red, Al in green, Sr in blue, and Ti in yellow.

To fabricate the memristor devices, Pt electrodes with a typical area of $150 \times 150\ \mu m^2$ are deposited on the LAO film using magnetron sputtering through a shadow mask, and Al wires are bonded to the interface using a wire bonder that can locally break through the ultrathin insulating LAO layer. A Keithley 4200 semiconductor characterization system is used to perform the resistance switching measurements. In the memristor, the metal Pt, which has a very large work function, and the conducting region near the LAO/STO interface serve as the top and the bottom electrodes, respectively [Fig. 1(a)]. The Al electrode reliably forms Ohmic contact with the bottom electrode, while the Pt/LAO/STO heterojunction exhibits high resistance (see the Appendix for details).

III. EXPERIMENTAL RESULTS

As shown in Fig. 3(a), the highly resistive initial resistance state (IRS) of the Pt/LAO/STO heterojunction exhibits significant rectification at room temperature in a voltage sweep from −4 to +4 V, indicating that the LAO layer retains its expected insulating characteristics. The rectifying behavior is similar to a recent report on a diode based on the LAO/STO interface with Au electrodes [40]. However, in our devices, this pristine state can be transformed into a switchable state using a simple reverse voltage sweep to −4 V. In the regime of negative bias,

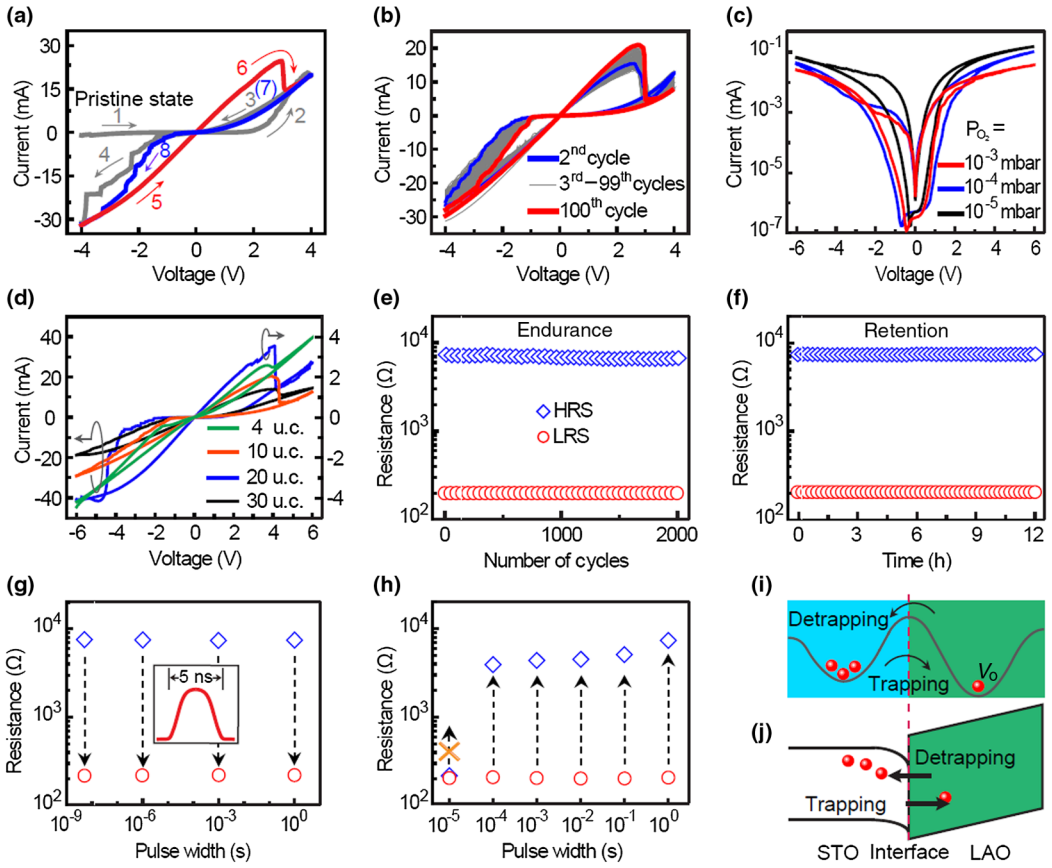

FIG. 3. (a) Forming process (voltage sweeps 1–4) transforms the device into the switchable states (sweeps 5–8). The red and the blue lines represent the LRS and HRS, respectively. The arrows mark the directions of the sweeping voltage. (b) After the forming process, the bipolar resistance switching is very stable during the successive voltage sweeps. (c) Reliable bipolar resistance switching, illustrated as absolute values of current as a function of voltages, can be observed in the devices with 10-u.c. LAO grown at different oxygen pressures. The *y* axes of (a)–(c) share the same label and unit. (d) Bipolar resistance switching in the memristors made of LAO films with different thickness (4 to 30 u.c.). (e),(f) The endurance and the retention data, respectively, with a readout voltage of 0.2 V. (g) Write speed can be as fast as 5 ns. (The pulse shape as recorded by an oscilloscope is shown in the inset.) Before the writing operations, voltage pulses of +4 V with a pulse width of 1 s are used to set the device to the HRS, and −4 V pulses with different pulse widths are applied to obtain the LRS. (h) Erase takes more than 100 μs. Voltage pulses of +4 V are used to accomplish the transition from the LRS to HRS. (i) Schematic illustrating the electric-field-induced trapping and detrapping of positively charged oxygen vacancies across an asymmetric energy barrier at the LAO/STO interface. (j) Schematic band diagram of the LAO/STO interface.

notable current fluctuations are observed that prelude the stable RS operations with bipolar switching *I-V* loops. Since the top electrode area is quite large ($150 \times 150\ \mu m^2$), the voltage-induced modification of transport may not be homogeneous. The characteristics of the bipolar switching loops, in particular the fact that a negative bias switches the device into the low-resistance state (LRS), resemble the results reported on Pt/STO/Nb:STO heterojunctions, where the motion of oxygen vacancies is involved [34]. In our devices, the LRS branches are linear and Ohmic, while the high-resistance state (HRS) branches exhibit a nonlinear rectifying behavior. Figure 3(b) shows the representative switching data of 100 cycles, which suggests that the Pt/LAO/STO memristor is very stable during successive voltage sweeps. The typical ON/OFF resistance ratio at a readout voltage of 0.2 V is close to 100, holding promise for practical memory devices.

Furthermore, we observed reliable memristor operations in devices synthesized with a wide range of oxygen growth pressures. Figure 3(c) shows the *I-V* switching loops of devices made of 10-u.c. LAO films grown at different oxygen pressures from 10^{-5} to 10^{-3} mbar. In general, the Pt/LAO/STO heterostructure is more resistive if the LAO film is deposited at high oxygen pressures, which corresponds to much lower currents in the CPP transport measurements. Growth with low oxygen pressures reduces the formation energy of oxygen vacancies, rendering the interface more conductive. Besides the memristors made of 10-u.c. LAO grown at 10^{-6} mbar, we test the performance of devices grown at other oxygen pressures, and the detailed data on a typical sample grown at 10^{-3} mbar can be found in the Appendix. We also examine the performance of devices made of LAO films with different thicknesses from 4 to 30 u.c., and all

devices exhibit reliable bipolar resistance switching behaviors [Fig. 3(d)].

During the operation of the LAO/STO memristors, the HRS and LRS can be reversibly and reproducibly obtained by applying voltage pulses of +4 and −4 V, respectively. The write (from HRS to LRS) and erase (from LRS to HRS) operations exhibit good endurance and consistent performance during more than 2000 operation cycles [Fig. 3(e)]. Furthermore, both the HRS and LRS are nonvolatile with retention of more than 12 h [Fig. 3(f)]. The demonstrated good retention and endurance characteristics are essential not only for memory applications but also for exploring the underlying switching mechanism.

To investigate the write speed, we apply +4-V pulses of 1 s to set the device to the HRS and then −4-V pulses with different pulse widths to obtain the LRS. Figure 3(g) shows that 5-ns electric pulses can successfully accomplish the write operation, and there is negligible dependence of the LRS resistance on the pulse width. We also find that all the devices examined in this work can be written with 5-ns pulses, and future experiments with shorter pulses are needed to investigate in detail the dependence of device speed on the device conditions. However, the erase operations need longer pulses; i.e., the transition from the LRS to HRS cannot be accomplished if the pulse is shorter than 100 μs [Fig. 3(h)]. Although the erase time can be improved to 1 μs if we use a higher voltage of 9 V, the asymmetry of switching speeds at different states is quite significant and its origin warrants further investigation.

Since oxygen vacancies are the mostly cited defects in LAO/STO heterostructures and they are known to significantly affect the CIP junction transport, we hypothesize that the device operation is closely related to the migration of oxygen vacancies across the LAO/STO interface as well as the subsequent movements within the ultrathin LAO layer. This idea is illustrated in the schematic in Fig. 3(i). In fact, the scenario of electric-field-driven drift of charged oxygen vacancies is often cited to explain the bipolar resistive switching observed in a wide range of transition-metal oxides [32,34,41–44]. The formation energy of oxygen vacancies is quite low in STO, and its presence cannot be excluded even in LAO/STO samples grown at high oxygen pressures (e.g., 10^{-3} mbar in our experiments) [18,45]. Oxygen vacancies can also exist in LAO, but the associated formation energy is much higher than that in STO [45,46]. The activation energy for oxygen-vacancy diffusion is only 0.75 eV in STO, whereas it is 2.2 eV in LAO [45]. It is well known that self-doped STO grown in low oxygen pressures possesses a high density of oxygen vacancies and is highly conducting [47,48]. In contrast, the as-grown LAO layer does not have extended oxygen vacancies and remains insulating, which is the reason why the pristine state of the Pt/LAO/STO junction shows a high resistance with tunneling characteristics [Fig. 3(a)]. However, a negative bias on the top Pt electrode creates an intense electric field that can move the positively charged oxygen vacancies from the STO side into the LAO layer and presumably causes the abrupt increases of current shown in Fig. 3(a).

The mobility of oxygen vacancies in STO is higher than those of most other perovskite oxides, and the diffusion coefficient can reach 10^{-4}–10^{-5} cm^2/s at high temperatures [49]. Although the diffusion of oxygen vacancies is slow at room temperature and can hardly move beyond 1 nm under the random walk condition, their mobility can be much higher under the influence of a high electric field [34]. Particularly, in our Pt/LAO/STO heterostructures, 1 V on the top Pt electrode corresponds to an enormous electric field of 2.6 MV/cm across 10 u.c. of LAO. Using micro-x-ray fluorescence mapping, Janousch and co-workers observed the distribution and the migration path of oxygen vacancies, and the electric field in their experiments is only on the scale of 10^5 V/cm [50]. As shown in Fig. 3(j), very short voltage pulses on the Pt electrode in our device can set the device because the LAO layer is extremely thin and the oxygen vacancies only need to migrate across the LAO/STO interface to accomplish the forming process, realizing the LRS. Besides the applied bias, the internal field within the LAO layer is a function of several factors, including the film thickness, electrode type, and even surface absorbates [16,51–57]. This built-in field may contribute to the asymmetry of the energy barrier for the migration of oxygen vacancies [Fig. 3(i)], which may be responsible for the fact that the write operation is several orders of magnitude faster than the erase one [Figs. 3(g) and 3(h)]. We should also note that the switching operation is a dynamic many-body process where electronic barrier height can be changed by electric field and locations of defects [58]. In our device, the accumulation of charged oxygen vacancies near the LAO/STO interface during the write operation can slow down their subsequent return during the erase operation as a result of the electrostatic repulsion between the charged vacancies. The dynamics of the switching operations can be quite complex, which warrants further investigation.

In a control experiment, we also fabricate devices on bare oxygen-deficient STO substrates with a configuration identical to the LAO/STO case. We anneal a piece of STO substrate with dimensions of $5 \times 5 \times 0.5$ mm^3 in the PLD chamber at 800 °C and 10^{-6} mbar for 20 min. As shown in the R-T curve in Fig. 4(a), the reduced STO shows a typical metallic behavior. This behavior is expected, as the oxygen vacancies in reduced STO donate electrons to the Ti 3d band, leading to metallic conduction [59]. We deposit Pt and Al electrodes on the reduced substrate [Fig. 4(b)], but we do not observe a notable resistance switching in the device [Fig. 4(c)]. Thus, we conclude that STO alone cannot give the observed resistance switching in the Pt/LAO/STO heterostructure, and this control experiment underscores the indispensable role of the LAO layer in the

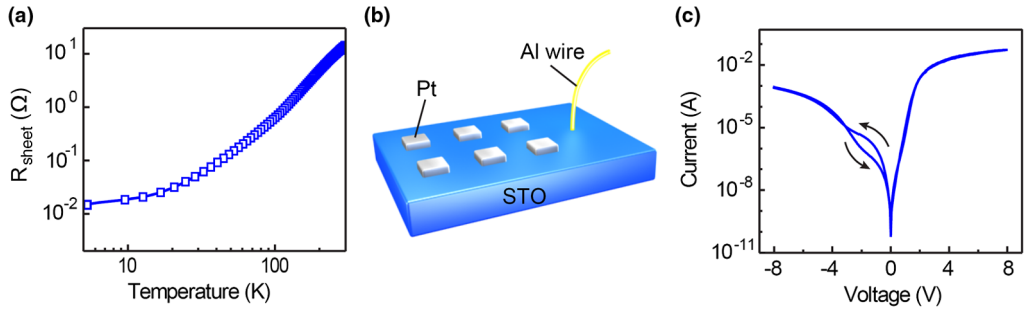

FIG. 4. (a) Sheet resistance vs temperature data measured on the reduced STO substrate. (b) Configuration of a device that has the same types of metal contacts but without the LAO layer. (c) Current (absolute values) vs voltage loop measured on the device. Even though the voltage scanning range is larger than what is used in the measurements of Pt/LAO/STO heterostructures, there is negligible hysteresis.

operation of the Pt/LAO/STO memristors. A recent theoretical study also pointed out the possibility of room-temperature redox reaction at the LAO surface involving oxygen vacancies [60], which may also contribute to memory effect.

To further shed light on the role of the ultrathin LAO layer, we investigate the temperature dependence of the *I-V* data of the IRS, and the results are shown in Fig. 5(a). In these experiments, a smaller voltage range is used to avoid switching of the Pt/LAO/STO heterostructure. To fit the data, we use the Brinkman-Dynes-Rowell (BDR) model, which is applicable for direct tunneling junctions with asymmetric energy barriers [61]. In this model, the voltage dependence of tunnel conductance $G(V) = dI/dV$ can be written as

$$\frac{G(V)}{G(0)} = 1 - \left(\frac{A_0 \Delta\phi}{16\phi_{\text{ave}}{}^{3/2}}\right)\text{eV} + \left(\frac{9}{128}\frac{A_0^2}{\phi_{\text{ave}}}\right)(\text{eV})^2, \quad (1)$$

where A_0 is a constant, ϕ_{ave} is the average barrier height, $\Delta\phi$ is the discrepancy of barrier heights at the two interfaces of the junction, $G(0) = (3.16 \times 10^{10}\phi_{\text{ave}}{}^{1/2}/d) \times \exp(-1.025 d\phi_{\text{ave}}{}^{1/2})$, and d is the barrier thickness that can be taken as the thickness of the 10-u.c. LAO layer. Figure 5(a) shows an excellent agreement between the experimental data and the model. From the fitting, we derive values of ϕ_{ave} and $\Delta\phi$ at room temperature as 0.516 and 0.443 eV, which correspond to two energy barriers of 0.295 and 0.738 eV for tunneling electrons in the Pt/LAO/STO heterojunctions [marked as ϕ_1 and ϕ_2 in Fig. 5(b)]. Recently, using x-ray photoelectron spectroscopy, Qiao and co-workers measured a conduction-band offset of about 2.8 eV at the LAO/STO interface [62], which is much larger than the deduced barrier height in our heterostructures. However, some first-principles calculations suggest that the energy barriers in metal/LAO/STO heterostructures are much reduced as a result of the metal overlayers [56], and significant modulations of the work function were also detected by *in situ* Kelvin-probe measurements at the LAO/STO polar interfaces [63]. To account for the thickness uncertainty in the LAO layer as suggested by the TEM images in Fig. 2, we carry out data fitting for a range of LAO thickness from 7 to 12 u.c., and the derived barrier heights are shown in Fig. 5(c). As expected, in order to produce the same level of conduction, the barriers have to be higher when the LAO layer is thinner. Theoretically, the heights of the Pt/LAO and the LAO/STO barriers calculated for such heterostructures show a slight dependence on the electric displacement field [56]. Nevertheless, the comparison of our experimental

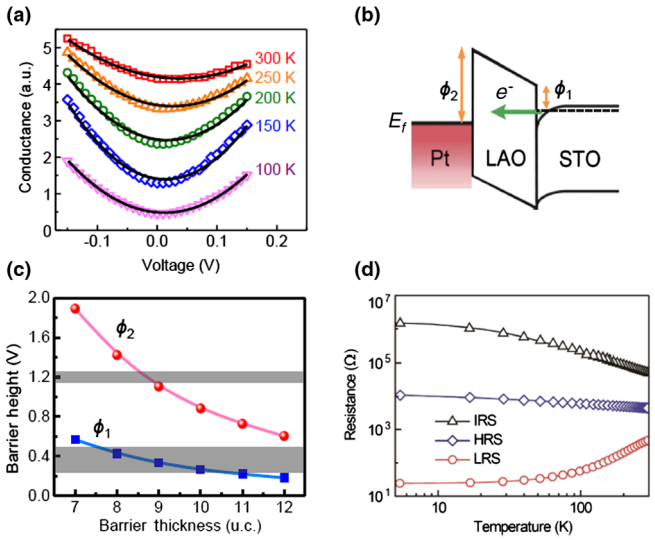

FIG. 5. (a) Junction conductance vs voltage data for the pristine state (IRS) measured at different temperatures. The black lines are the theoretical fitting results using the BDR model expected for direct tunneling junctions. (b) Schematic energy diagram of the Pt/LAO/STO heterojunction where the two asymmetric barriers are labeled as ϕ_1 and ϕ_2. (c) Derived barrier heights plotted as a function of the LAO thickness. The two gray belts mark the ranges of barrier heights calculated in Ref. [56]. (d) Temperature dependence of the memristor resistance at different states. During the measurements, a constant voltage bias of 0.15 V is used. Overall, the forming and switching processes of the memristor correspond to reversible transitions between tunneling and Ohmic transport characteristics of the Pt/LAO/STO heterojunctions.

data with the theoretical prediction shown in Fig. 5(c) suggests that it is more appropriate to treat the thickness of the LAO barrier as 8.5 u.c. instead of the nominal 10 u.c.

This tunneling characteristic of the junction transport is consistent with the fact that LAO is a conventional band insulator with a wide band gap of 5.6 eV. It is noteworthy that the direct tunneling across the heterojunction suggests the absence of excessive electronic trapping during device operations, which can be ascribed to the high crystalline quality of the heterojunction. In the forming process with the negative voltage bias, positively charged oxygen vacancies in STO are driven into the LAO layer, creating an extended defect band within the band gap of LAO. If the defect band aligns with the Fermi level of Pt, a metallic transport through the junction can be achieved, which is retained even after the external voltage bias is removed, giving rise to the nonvolatile LRS. We measure the temperature dependence of different resistance states, and indeed, we find that both the IRS and HRS of the heterojunction show an insulating behavior, whereas the LRS exhibits a clear metallic nature [Fig. 5(d)]. In general, the HRS exhibits lower resistance than the IRS, and its exact transport mechanism requires further investigation. Overall, the RS operation of our Pt/LAO/STO heterostructures is accompanied by concurrent reversible insulator-metal transitions.

It is noteworthy that the conducting layer near the LAO/STO interface has a much lower electron density than conventional metallic bottom electrodes. As a result, the effective Fermi-Thomas screening length can be quite long. The long screening length leads to an incomplete screening of the electrical field by the conducting electrons and a penetration of the unscreened electric field into the STO side that is effective in causing the charged oxygen vacancies to drift across the LAO/STO interface. Furthermore, because the LAO layer is only a few unit cells thin, a small number of migrated oxygen vacancies is expected to trigger a significant effect in the CPP transport of the Pt/LAO/STO heterostructures.

IV. FIRST-PRINCIPLES CALCULATIONS

Can migrated oxygen vacancies really form defect states at the Fermi level in the thin LAO layer? To answer this question, we perform first-principles density-functional-theory (DFT) calculations using the Vienna *ab initio* simulation package (VASP) [64,65] on the LAO/STO systems with different oxygen-vacancy concentrations in LAO. More details can be found in the Appendix. We first calculate the layer-resolved density of states (LDOS) of a 6-u.c. LAO/8-u.c. STO interface and apply the Hubbard U correction to account for the on-site Coulomb interaction.

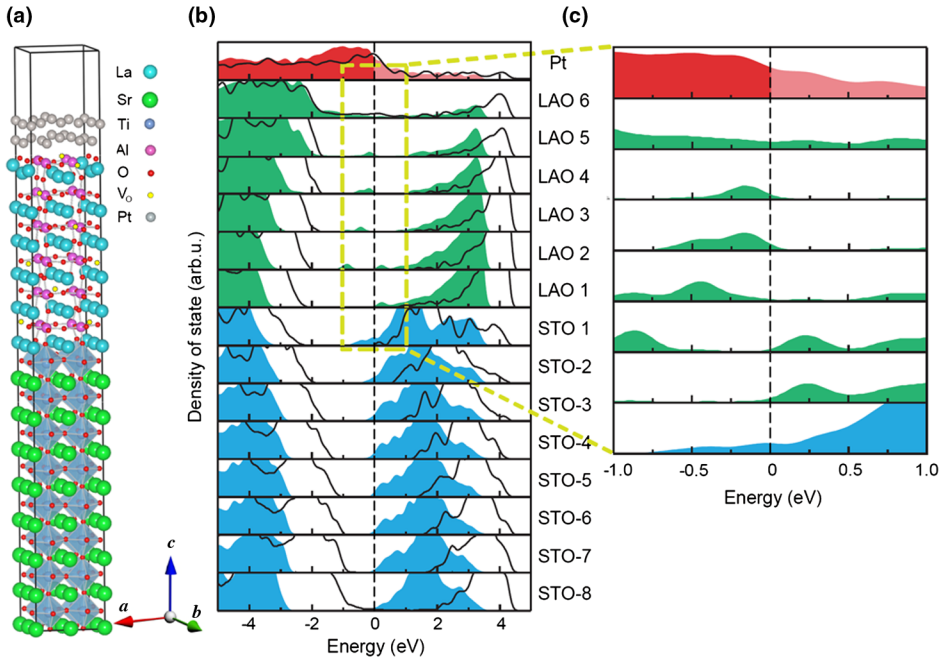

FIG. 6. (a) Simulated structure of the 2×2 supercell of 1-u.c. Pt/6-u.c. LAO/8-u.c. STO or $Pt_1/(LAO)_6/(STO)_8$ with oxygen vacancies. In this model, we remove one individual oxygen atom from each LAO layer, corresponding to six oxygen vacancies in the (2×2) supercell. Accordingly, the concentration of oxygen vacancies is $6/72 \approx 8.3\%$. (b) LDOS of the $Pt_1/(LAO)_6/(STO)_8$ system for the "pristine" LAO (without any oxygen vacancy, shown as the black curves) and the "formed" state after incorporation of oxygen vacancies in LAO (filled areas). With the pristine LAO, the Fermi level of Pt falls in the band gap of the LAO, leading to the tunneling transport of the IRS. On the other hand, oxygen vacancies help to produce an extended defect band in the LAO that aligns with the Fermi level of Pt, giving rise to the metallic LRS of the memristor. (c) Close-up view of the LDOS near the Fermi level.

The calculations, in general, reproduce the earlier results of the 2D electron system at the LAO/STO interface [66].

Figure 6(a) shows the simulated structure of a 2×2 supercell of 1-u.c. Pt/6-u.c. LAO/8-u.c. STO, where we remove one individual oxygen atom from each LAO layer, corresponding to an oxygen-vacancy concentration of approximately 8.3%. All the oxygen vacancies are located in the AlO_2 layers as a result of the lower formation energy here, as compared to the LAO layers [67]. When there is no oxygen vacancy in the LAO layers, there is no density of states in most LAO layers [black lines in Fig. 6(b)], and electrons cannot transport between the Pt contact and the conducting interfacial STO layer; in this case, the Fermi level of Pt falls into the band gap of LAO, resulting in the tunneling transport across the heterojunction, which is consistent with the transport characteristics of the IRS (Fig. 5). On the other hand, when oxygen vacancies are introduced, the defect-related energy states are generated in the band gap of LAO, and the defect-derived band aligns with the Fermi level of Pt [Fig. 6(c)]. This scenario of metallic junction transport as a result of the formation of a defect-related quasiconduction band is consistent with a recent report on metal/LAO/Nb-STO heterostructures [68]. However, in the thick LAO films on the scale of 100 nm, the defect states exist at roughly 2 eV below the conduction-band edge [68,69], which was also proposed in a first-principles study [46]. In contract, in our Pt/LAO/STO heterostructure with an ultrathin LAO layer, the electronic band structure is modified in a different way by the oxygen vacancies. As shown in Figs. 6(b) and 6(c), the defect-derived states completely erase the band gap in the first LAO unit cell below Pt, whereas the Fermi level moves up into the conduction band in the few LAO unit cells near STO. Here, we have not considered the formation of extended defect complexes, such as vacancy chains and edge and screw dislocations, which are common in transition-metal oxides [34]. Nonetheless, it is clear that the existence of oxygen vacancies and their field-induced migration bears significance on the CPP transport of Pt/LAO/STO heterostructures, and even a small amount of vacancies can induce a drastic transition in the junction transport from tunneling to Ohmic characteristics.

V. DISCUSSION AND CONCLUSION

In this work, we have demonstrated a metal-oxide-oxide RS device based on Pt/LAO/STO heterostructures, and the mechanism involving field-induced migration of oxygen vacancies across the oxide interface can qualitatively explain the observed switching between metallic and insulating states. However, we should be cautious and stress that our data interpretation pertains only to the CPP transport, where the migration of oxygen vacancies into the ultrathin LAO layer could be laterally inhomogeneous. Thus, even small patches containing sufficient oxygen vacancies on the nanometer scale may form localized conduction regions and short the perpendicular current, giving rise to the observed insulator-to-metal transition. On the other hand, isolated patches of oxygen vacancies may not contribute significantly to the usually reported CIP transport if the samples are properly oxidized during the growth process.

Since the resistance switching effect hinges on the drift of oxygen vacancies near the LAO/STO interface and in the LAO layer, the different memory states should be correlated with the CIP transport characteristics of the electron gas. Under an applied gate bias, the unscreened electric field is effective to attract or repel the charged oxygen vacancies inside the STO substrate, relative to the LAO/STO interface. Figure 7(a) shows the schematic of the device we use to explore the hypothesized correlation between the CIP and the CPP transport properties. In the device, the length of the Pt electrode is 150 μm, covering the majority part of the 190-μm-long channel between the two inner Al electrodes. A negative bias on the Pt electrode will move the positively charged oxygen vacancies from the deeper region of the STO substrate toward the interface, and the concentration of oxygen vacancies in the region increases. Consequently, the electrons donated by oxygen vacancies contribute to the conduction and reduce the sheet resistance measured in the CIP transport. In addition, the conversion of part of the LAO layer to metallic further facilitates the CIP conduction. Vice versa, the application of a positive bias can drive the oxygen vacancies back into the deeper part of the STO substrate,

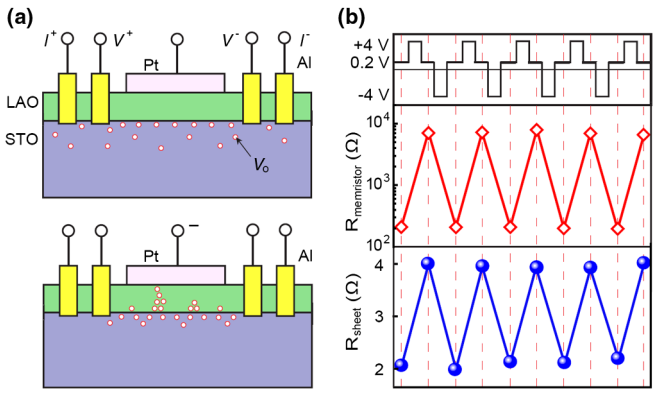

FIG. 7. (a) Schematic diagram of the experimental setup for monitoring the sheet resistance of electron gas after switching the memristor into different resistance states. As depicted in the figure, the four-point configuration with bonded Al electrodes is used to record the lateral sheet resistance. When a negative voltage bias is applied to the top Pt electrode, oxygen vacancies are driven toward the interface, which should not only render the LRS but also decrease the sheet resistance of the electron gas in STO. The reverse effect occurs when a positive bias is applied. (b) "In-plane" sheet resistance of the electron gas changes accordingly when voltage pulses of ± 4 V are applied to the top Pt electrodes that concurrently switch the "out-of-plane" memristor into the HRS and LRS. For the CIP transport, the readout voltage is 0.2 V.

recovering the previous high sheet resistance of the interface. Indeed, experimentally, we find that the sheet resistance can be modulated accordingly when the memristor is switched into different resistance states by voltage pulsed of ± 4 V, and the modulation is fully reversible [Fig. 7(b)].

The inhomogeneous character of the CPP transport is ubiquitous in RS devices under the stimulus of an intense electric field. The extrinsic sources of such inhomogeneity in our Pt/LAO/STO devices can be terrace steps on STO substrates, incomplete coverage of the LAO layer, local nonstoichiometry in composition, clusters of structural dislocations, and so on. Inoue and co-workers recently proposed a scenario of an "electric faucet" where current only flows through such faucets at the interface at the LRS and the faucets are closed at the HRS [70]. This scenario of localized conduction is consistent with our observation in Fig. 3(d) that shows that the switching voltage depends little on the thickness of the LAO layer. Furthermore, because of the localized nature of such an electric faucet, the current in the CPP transport does not scale with the size of the top Pt electrode. We schematically illustrate the mechanism of resistive switching of our Pt/LAO/STO devices in Fig. 8. In the forming process, the applied electric field moves the charged oxygen vacancies into the LAO layer and conducting filaments form. In the subsequent RS operations, only the electric faucet opens or closes at the filament or electrode interface, giving rise to the LRS or HRS.

RS has been reported in heterostructures made of many different oxides, and reliable operations can be achieved in epitaxial, textured, polycrystalline, or even amorphous

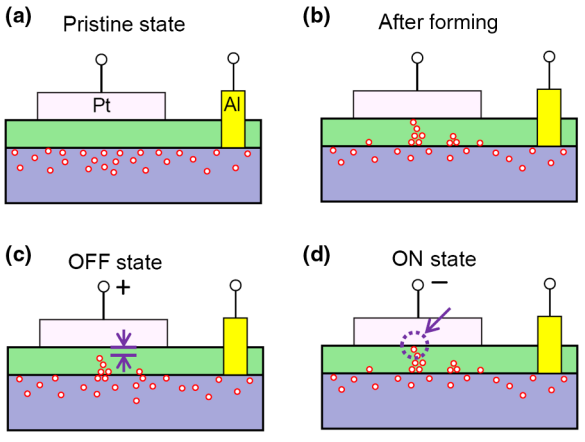

FIG. 8. Schematic illustration of the RS mechanism in Pt/LAO/STO devices. (a) In the pristine state, the as-grown LAO layer is insulating, and the CPP transport is of the tunneling type. However, (b) after the forming process, conducting filaments of oxygen vacancies form across the LAO layer, giving rise to the Ohmic transport. As shown in (c) and (d), the close and open actions of the "electric faucet" near the filament or electrode interface are responsible for the HRS and LRS. In (c), the arrows mark the effective thickness of the LAO layer that remains as an insulating barrier. The region of the electric faucet is highlighted in (d).

materials. It helps to elucidate the mechanism by comparing the Pt/LAO/STO devices studied here with commonly reported capacitor-type RS structures made of transition-metal oxides such as TiO_2 [32,33]. In such devices, the switching oxide layers are usually at least 1 order of magnitude thicker than the LAO layers in our devices, and they are sandwiched between two metal electrodes. Particularly, TiO_2-based memristors contain vertically stacked insulating TiO_2 and oxygen-poor TiO_{2-x} regions. During the device operation, the positively charged oxygen vacancies drift in the applied electric field, shifting the boundary between the two regions, leading to the switching of the device resistance. On the other hand, in the LAO/STO heterojunctions reported here, the STO substrate is the "reservoir" for oxygen vacancies, and the migration of oxygen vacancies across the "fixed" LAO/STO interface enables the switching operations.

The electronic band structure and the ultrathin nature of the LAO layer in our Pt/LAO/STO devices lead to switching characteristics different from the previously reported memory devices using thick LAO films on the scale of 50–150 nm [68,71,72]. By fitting our data to the BDR model, we prove that the transport across the as-grown LAO layer with a thickness of a few unit cells follows the direct tunneling mechanism. In a recent study of Pt/STO (4–5-nm)/Pt junctions, it is proposed that the observed memory effect and negative differential resistance are correlated with resonant tunneling [58]. It should be noted that such quantum mechanical tunneling of electrons is forbidden in junctions with thick switching oxide layers. Besides the barrier thickness, the characteristics of defects, either intentionally or unintentionally generated in the thin-film deposition process, significantly affect the physical properties and the operation of the RS devices. As reported by several previous experiments on LAO-based devices, a forming process is required to generate defects and to enable the subsequent switching in the RS devices [71,72]; in contrast, Liu and co-workers proposed that a defect-related quasiconduction band already exists in the LAO layer and the device operation does not need a forming process [68]. In addition, because of the ultrathin nature of the LAO layers in our Pt/LAO/STO heterostructures, the forming voltage used in our experiments is much smaller than those required in experiments with thicker LAO films [71,72]. Another difference in our device characteristics is that we observed the abrupt stepwise increase of current in the forming sweep, as shown in Fig. 3(a), and its correlation with the formation of atomic-scale conduction filaments warrants further investigation [73].

The migration of charged oxygen vacancies is the mostly cited mechanism responsible for the RS behavior observed in a wide range of sandwich-type oxide-based devices [34,74–78]. However, as proposed by Liu and co-workers, the trapping or detrapping of electrons in the defect-derived quasiconduction band in 150-nm-thick

LAO films can lead to the overlap of wave functions and the reversible insulator-metal transitions [68]. In fact, Simmons and Verderber speculated in 1967 that injected ions can introduce a broad band of defect states within the band gap of insulators and that the trapping or detrapping of electrons accounts for the memory effects [79]. A similar mechanism was recently employed to explain the RS behaviors in TiO_2-based devices [80]. In contrast to the works on thick oxide films in literature, the electric field across the ultrathin LAO layers in our Pt/LAO/STO heterostructures is on the scale of MV/cm, which is high enough to trigger the drift of charged oxygen vacancies. Such electric-field-induced migration of oxygen vacancies between bistable configurations was also proposed by Bark and co-workers to explain the hysteretic response of switchable polarization in their piezoresponse-force-microscopy study of LAO/STO heterostructures [81]. Additionally, it is noteworthy that the good oxygen-diffusion ability reported for Pt facilitates the electric-field-induced drift of oxygen vacancies in our Pt/LAO/STO heterostructures [82].

In summary, we have shown that oxide heterostructures enabled by the epitaxial synthesis controlled on the unit-cell level can work as promising memristors and that the active LAO layer can be as thin as 4 u.c. (approximately 1.5 nm). In turn, our data provide valuable information on the field-induced migration of oxygen vacancies in ultrathin oxide heterostructures as well as the mechanism of reversible transition between tunneling and Ohmic characteristics in the CPP junction transport. In the pristine state, the Pt/LAO/STO heterojunction exhibits direct-tunneling-type characteristics with the interfacial energy barriers, matching well the theoretical prediction. We propose that oxygen vacancies in STO, whose role remains controversial in the CIP transport in LAO/STO heterostructures, drift under the intense electric field in the CPP transport and enable the RS operation in our Pt/LAO/STO heterostructures. In addition, our first-principles calculations that consider the influence of the metal overlayer on the electronic band structure of the LAO/STO interface shed light on the experimental results. More importantly, the nonvolatile memory demonstrated here is ready for integration with other existing interface-based FET devices in constructing oxide electronics on the circuit level with complementary memory and logic functions.

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APPENDIX

Details of first-principles calculations.—A plane-wave basis set and projector-augmented-wave potential as implemented in VASP are employed. All the calculations are based on DFT within the generalized-gradient approximation. During the structure relaxation, the ion positions and the out-of-plane lattice constants are fully relaxed with the constraint that the in-plane lattice constants are fixed to the theoretical value of STO (3.93 Å). The lattice relaxations are considered as converged when the maximum Hellman-Feynman force acting on each atom is less than 0.01 eV/Å. Based on these fully relaxed structures, the electronic properties are calculated. In the electronic structure calculations, we use a converged plane-wave cutoff energy of 450 eV, together with a 0.2-eV Gaussian broadening. For the k-point sampling in the Brillouin zone, a well-converged $8 \times 8 \times 1$ Monkhorst-Pack grid is used for the perfect structures, while a $3 \times 3 \times 1$ Monkhorst-Pack

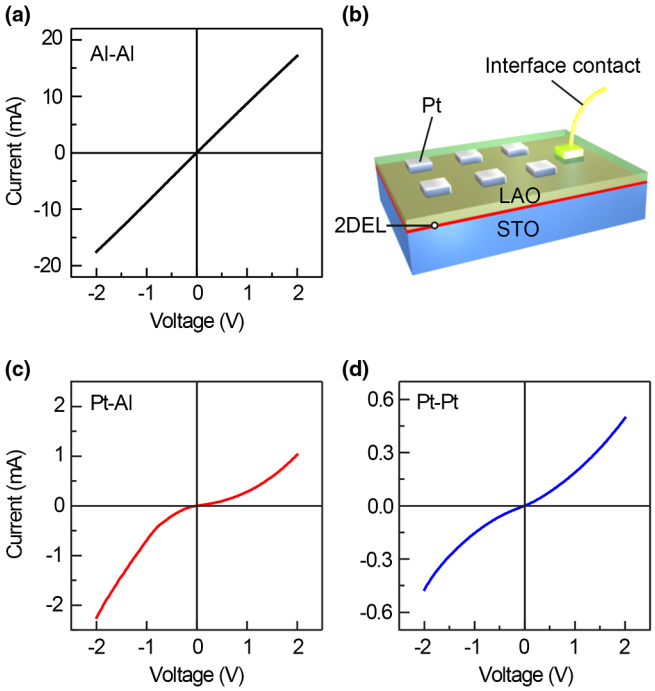

FIG. 9. Dependence of transport characteristics of the memristor on the electrode configurations. (a) The I-V curve between two Al electrodes exhibits Ohmic behavior. (b) Schematic view of a memristor device, where the conducting two-dimensional electron liquid (2DEL) near the LAO/STO interface serves as the BE, while Pt on LAO serves as the TE. (c) The I-V curve between Pt and Al electrodes shows diodelike rectifying nonlinear characteristics. (d) The I-V curve between two Pt electrodes shows symmetric nonlinear characteristics.

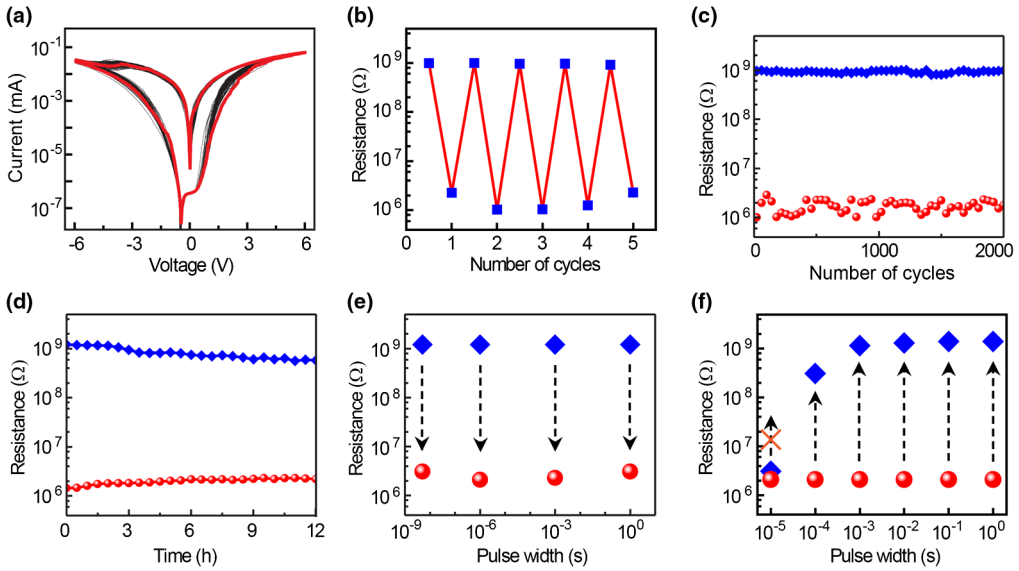

FIG. 10. Nonvolatile resistive switching of the LAO/STO memristors with LAO grown at a relatively high oxygen pressure of 10^{-3} mbar. (a) After the initial forming sweep, bipolar resistance switching is very stable during the 100 successive voltage sweeps. The red curve represents the 100th cycle. (b) The HRS and LRS can be reversibly and reproducibly obtained by applying voltage pulses of ± 6 V. The readout voltage is 0.2 V. (c) Good endurance and no performance degradation are observed after 2000 cycles of write and erase operations. (d) Both the HRS and LRS are nonvolatile with a retention of more than 12 h. (e) Write speed can be as fast as 5 ns. (f) Erase operation takes more than 100 μs. It is noteworthy that these characteristics are similar to the devices made at a relatively low oxygen pressure of 10^{-6} mbar.

grid is used for the 2×2 supercell containing oxygen vacancies. Since the DFT calculations often underestimate the band gap in the generalized-gradient approximation or local-density approximation, we apply the Hubbard U correction to account for the on-site Coulomb interaction. In order to have a more realistic description of the band gaps of the interface system, we use $U = 6$ eV for the Ti $3d$ electrons and 7 eV for the La $4f$ electrons.

Scanning transmission electron microscopy.—A cross-sectional sample of the Pt/LAO/STO stack is prepared for HAADF-STEM investigation by focused ion beam milling in a FEI Helios focused ion beam SEM. High-angle annular dark-field STEM images are acquired using an aberration-corrected Titan microscope operated at 300 kV, using a convergence semiangle α of 21 mrad and an acceptance semiangle β of 50 mrad.

Supplementary data.—Figure 9 shows the memristor configuration and the transport characteristics between different Pt-Al electrode combinations. Figure 10 shows the nonvolatile resistive switching of the LAO/STO memristor with LAO grown at an oxygen pressure of 10^{-3} mbar.

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